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GaAsFET Power Amplifier Stages up to 5 W for 10 GHz

The following article introduces two high-level output stages for 10 GHz. Both modules were developed by the author with a view to ease of copying and reliable long-term operation. Numerous examples of the 1W high-level stage have been running for some years (some of them installed on masts) and none has yet given rise to any problems.

1. INTRODUCTION

The last few years have seen the emergence onto the market of output GaAs FET's in the 5W range, which certainly do drain the "research budget" of a radio amateur, right down to the last penny. But "better 5 Watts in the GHz rucksack than a designer suit in the wardrobe". Thus the tried and tested existing circuit was expanded by a TIM 0910-4 from Toshiba, which was internally tuned to 50Ω. Five examples of the 5W version have been assembled so far. Long-term operation in the laboratory and utilisation by several competitors (figuratively left out in the cold and expeditions literally snowed up) have left the hope open that this high-level stage can also attain the operational reliability of the 1W version. In one example, at least, a faulty SMA relay triggered a ten-minute crash test with full power drive but open output. The transistor survived the experience, though the author was forced to part with the relay.

In spite of all efforts at reproducibility, I am obliged to admit that the cumulative total of the small tolerances in the component values and the assembly can eventually lead to significant individual deviations (-3 dB is normal) in the amplification and output power. But there is some comfort in the fact that, with patience, experience and good measurement facilities, a high-level stage can be trimmed to the rated values with a fine calibration using the "small disc method".

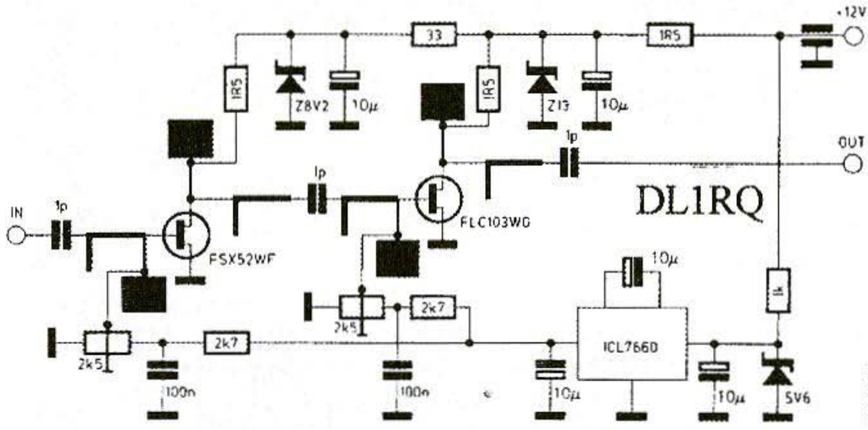


Fig.1: Circuit Diagram of the 1W Power Amplifier for 10 GHz

The following descriptions are intended to provide a stimulus to the interested radio amateur. No doubt further slight changes will occur as this concept is optimised further.

2. 1W HIGH-LEVEL STAGE FOR 10 GHz

2.1. Description

The wiring diagram (Fig.1) is comparable in structure to the author's two-part 5.7 GHz high-level stage, published in (1) and (2), down to the additional voltage inverter for the negative gate voltage. Good experiences with the reliable FSX52WF transistors (drive) and FLC103WG transistors (high-level stage) from Fujitsu led to trials at 10 GHz, which were immediately successful, although the FLC103WG is specified only for use up to 8 GHz by the manufacturer. 0805 model 1pF SMD capacitors were used as high-frequency coupling elements (2.0 mm. x 1.25 mm.). Research carried out only recently as part of a specialist project (3) showed that the SMD capacitors used by the author, with a series inductance of L_{Series} = 0.66 ±0.01 nH,

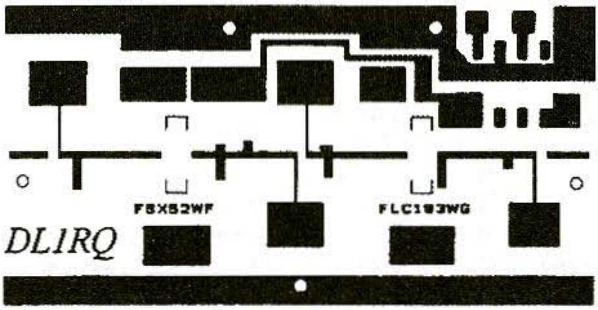


Fig.2: Board Layout of the 1W Version

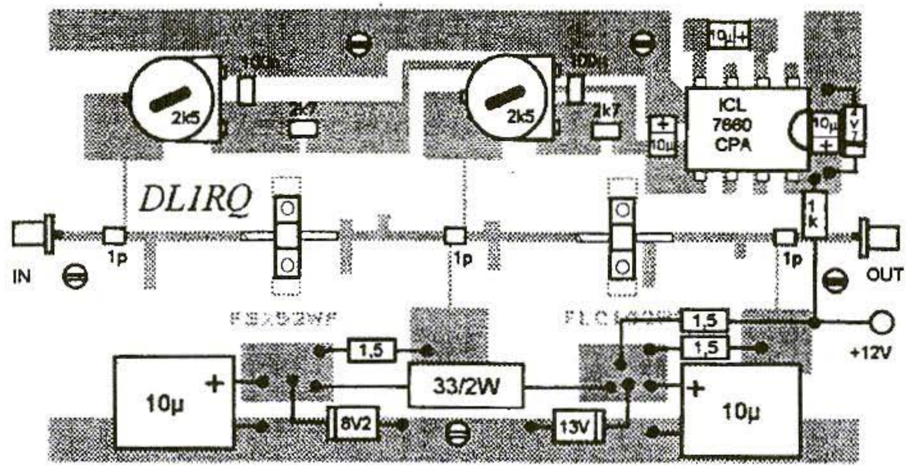


Fig.3: Component Layout of the 1W Version

differ from those components available by normal mail order, with L_{Series} = 0.72 ±0.02 nH. Unfortunately, the author was no longer in a position to identify the individual manufacturer. In any case, a rough calculation quickly shows that the series resonance frequency of these SMD capacitors lies around 6.0 GHz. So, at 10 GHz the coupling "capacitors" should be considered more as DC-disconnecting components with inductive behaviour. Naturally, this inductance clearly has an influence on the transformation by the calibration elements (at the cost of narrowing the band!).

The power supply was deliberately made simple. Stabilisation was provided through 1.3W Zener diodes, which simultaneously provided protection against overvoltage and false polarity. The 1.5Ω / 0.25W axial carbon film resistors fulfil their purpose as disconnection resistances and as safety resistances. A protective circuit in case the negative power supply failed was dispensed with following an involuntary 24-hour test without any minus voltage, which did not result in any damage to the semi-conductors.

2.2. Assembly

The assembly and board layout of an amplifier for microwaves are determined by two essential requirements:

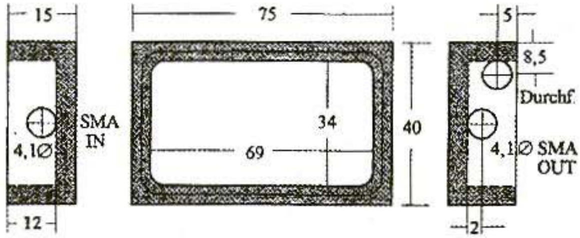


Fig.4: Dimensions for the Milled Aluminium Housing in mm

Durchf = Connectors

- The high-frequency transition from the earth surface of the board to the source flange of the transistor must be as close to ideal and as smooth as possible
- The extraction of the transistor's lost heat must be as close to ideal as possible

A board with a sandwich construction has proved itself as a way of being able to fulfil both requirements simultaneously. The layout (Fig.2) is etched onto an RT/Duroid D-5870 board measuring 68.5 mm. x 34 mm. x 0.25 mm.. After pre-tinning of the earth surface, the board is soldered onto a 1.0 mm. thick copper plate under high pressure. Next, two oval grooves 0.75 mm. deep are milled, using a 2.5 mm. diameter bore groove milling cutter, for the source flanges of the transistors. When the five 2.1 mm. diameter holes have been made for the board to be screwed into the housing and for the contacts to be connected up, and when the tracks have been tin-plated (or silver-plated), the board is assembled as far as the two 10µF electrical capacitors (on the drain side) and the transistors (Fig.3). In order to guarantee good heat transmission between the copper plate and the milled aluminium housing (Fig.4), some heat-conducting paste is smeared over the aluminium base in the vicinity of the transistors. To ensure good transition between the high-frequency section and the earth in the input and output areas, silver conducting lacquer can be smeared there (very sparingly, of course). The partly-assembled board is now incorporated into the suitably prepared aluminium housing and screwed down by five M2 brass screws. When the connections to the feed-through capacitor have been completed, it is already possible to check the DC function. For this purpose, the two trimmers are pre-set to a gate voltage of about - 1.5 V.

The trickiest stage in the procedure is the soldering of the GaAsFET into the milled grooves. To this end, the aluminium housing is first heated, with the

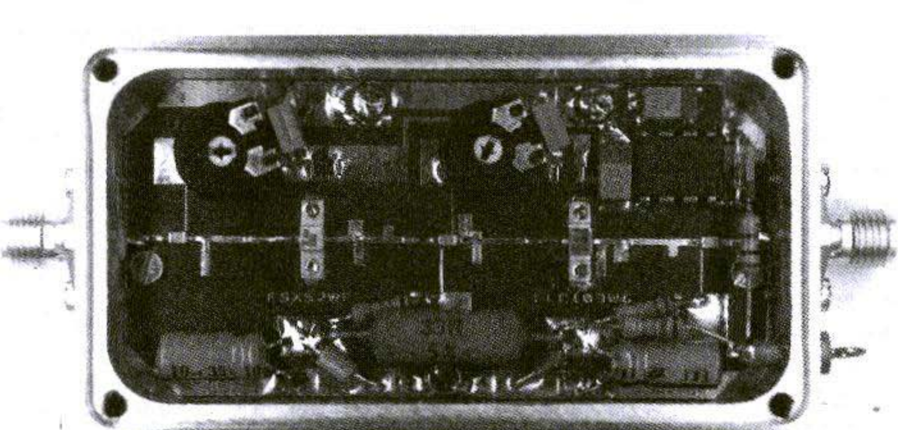


Fig.5: Example of a 1W Power Amplifier for 10 GHz

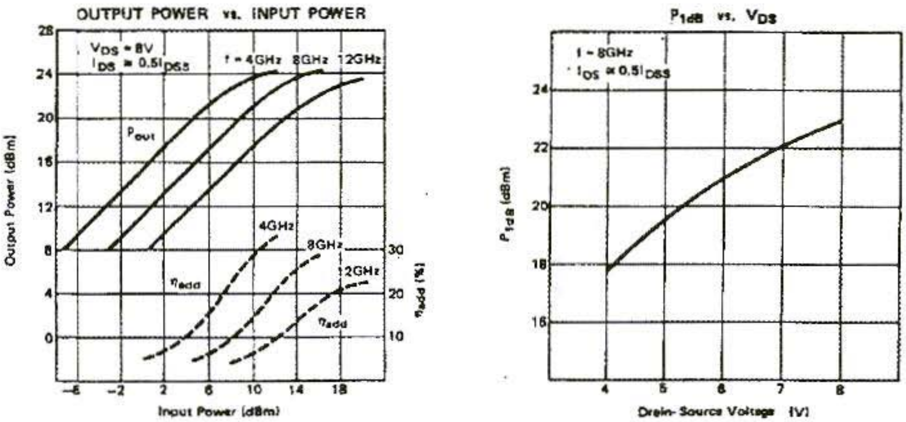


Fig.6: Power Data for the FSX52WF taken from the Fujitsu Data Sheet (5)

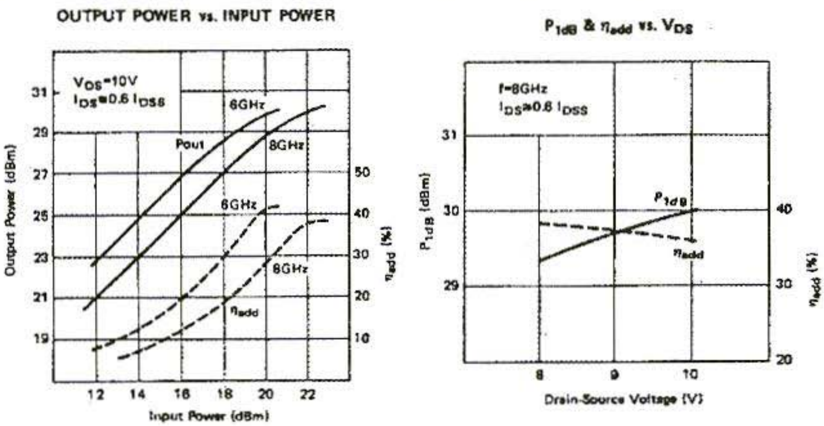


Fig.7: Power Data for the FLC103WG taken from the Fujitsu Data Sheet (5)

board inside it, to precisely 150°C. Each milled groove is then pre-tinned, using low-temperature solder with a melting temperature of 140°C. Excess tin is then removed using a de-soldering pump. The transistors are then placed in the grooves - all the relevant safety measures known must be taken. Normally, the tin binds very well with the gold-plated flanged base - something which can easily be tested by a visual check of the flanged bores. Naturally, this soldering process should be carried out as rapidly as possible. The housing is then immediately placed on a cold copper block or a large cooling body, so that the temperature quickly falls.

Drain and gate connections are soldered onto the stripline - all the relevant safety measures must be taken. The two 10µF capacitors on the drain side are fitted and the SMA flanged bushes are screwed on. The high-level stage is ready for fine calibration (Fig.5).

2.3. Calibration

First, the zero signal currents are set as follows:

For the FSX52WF at app. 70mA, this corresponds to a voltage drop of 105 mV, with a 1.5Ω protective resistor. For the FLC103WG, at app. 240mA, it corresponds to a voltage drop of 360 mV, with a 1.5Ω protective resistor.

With a 30mW drive at the desired frequency, an output of approximately 400mW (in the worst case) and of 1 Watt (in the ideal case) should be measurable. As already mentioned initially, the "small disc method" is normally of assistance. Small discs, measuring about 2 - 4 mm.², a few toothpicks to press down and push, a lot of patience and, above all, the greatest care in watching out for short-circuits

Typical Readings for the 1W Unit

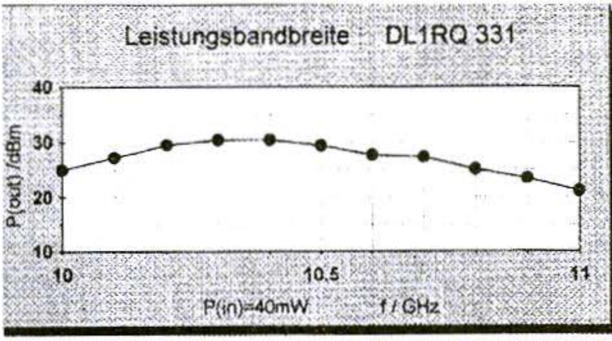


Fig.8: Power Bandwidth

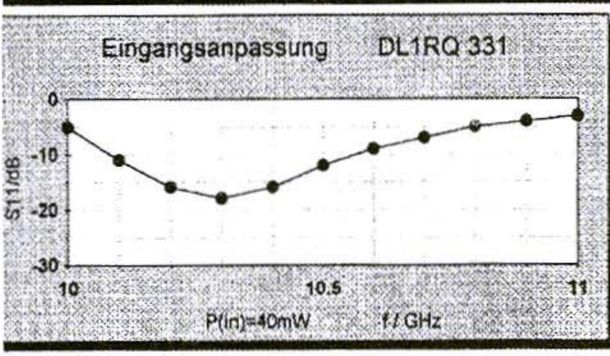


Fig.9: Input Matching

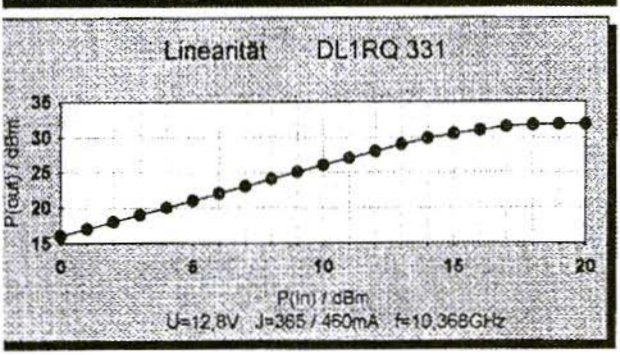


Fig.10: Linearity

will (hopefully) soon lead you to your goal. After calibration, an aluminium plate cover 1 mm. thick can be pressed into a matching edge milling. In the overwhelming majority of the high-level stages measured, almost no influence from the cover could be detected. Of course, there were just a few cases in which minimal self-excitation was detected when the cover was put on. This is seen as an astonishingly stable housing resonance, lying slightly above the calibration frequency, with a few milliwatts of power at the output. Even this undesirable oscillation disappeared with a low-powered drive. A strip of absorbent material about 5 mm. wide and about 10 mm. long, glued to the inside of the cover in the area above the FSX52WF, provided a reliable remedy here.

2.4. Data and Readings

A comparison of the output data from the semi-conductors (Fig.6 and Fig.7) with the readings from a typical high-level stage (Fig.8 - Fig.10) makes clear how successful the project is in practice.

3. 5W HIGH-LEVEL STAGE FOR 10 GHz

3.1. Description

The circuit diagram for the 5 Watt high-level stage (Fig.11) differs from the circuit diagram for the 1 Watt high-level stage due to the inclusion of the additional power pack with the

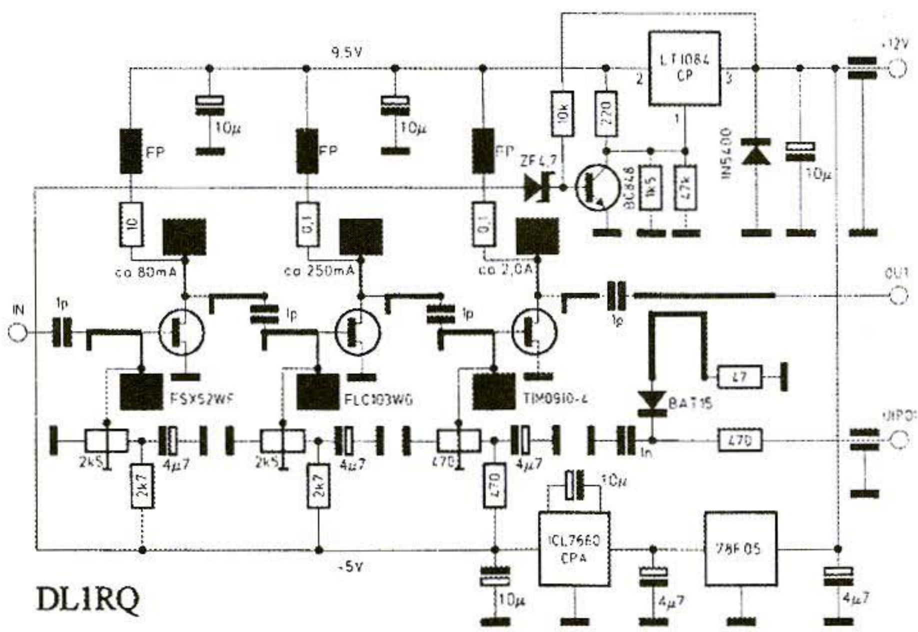


Fig.11: Circuit Diagram of 5W Power Amplifier for 10 GHz

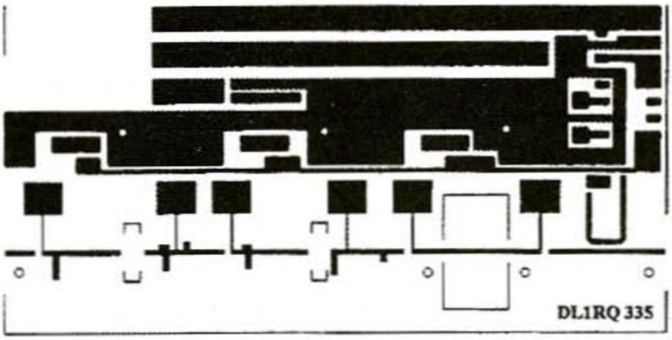


Fig.12: Board Layout of the 5W Version

TIM0910-4 Toshiba internally matched power GaAsFET and due to a more expensive power supply circuit, provided by DB6NT largely copied from (4). The LT1084CP 5-A low-drop regulator is permanently set to a drain voltage of 9.5 V, and is switched off through the BC848 transistor if the - 5 V voltage cuts out. The relatively high-resistance gate circuitry of the TIM0910-4 corresponds to a recommendation from the manufacturer. With high-frequency drive, it leads to an increase in UGS and thus to an artificial counter-coupling. In this way, undesirable oscillation can be avoided, in accordance with the manufacturer's recommendation. This explains the fall in the power consumption from app. 2.5 A without drive to app. 2.1 A with full drive. The first appearance of the gate current can also be detected in the linearity diagram (Fig.18) as a slight bend in the characteristic line at an output of app. 3 dBm. 2Watt. Cemented wire resistances of 10Ω or 0.1Ω are used as drain resistances. They have adequate inductance and the voltage drop on them can be made use of for the convenient measurement of the

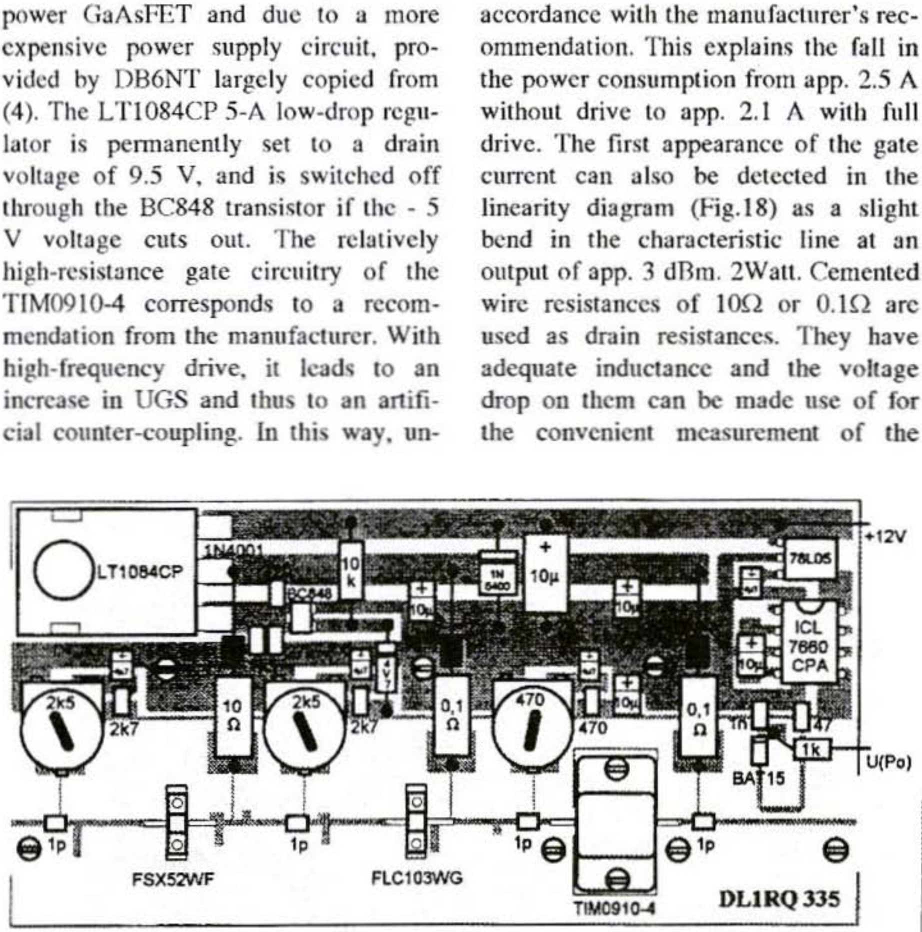


Fig.13: Component Layout of the 5W Version

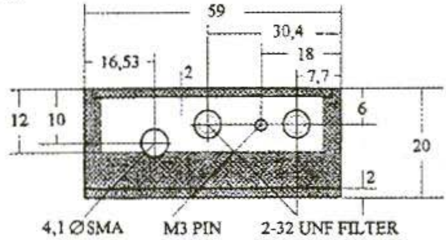


Fig.14: Dimensions of the Telemeter ZG4-2-N Housing in mm

drain current. The ferrite beads threaded on could be described as "hope beads", as they are connected with the hope that they contribute to the suppression of undesirable housing resonances. A Siemens directional coupler with a type BAT 15-098 low-barrier Schottky diode is provided for the monitoring of the output.

3.2. Assembly

There are some structurally determined differences between the assembly of the 5 Watt high-level stage and that of the 1 Watt high-level stage. The layout (Fig.12) is etched onto an RT/Duroid D-5870 board measuring 101.6 mm. x 50.8 mm. x 0.25 mm. (4 x 2 x 0.01 in.). The dimensions arise from the use of a finish-milled, nickel-plated type ZG4-2-N aluminium housing from Telemeter Electronic (6). Following the pre-tinning of the earth surface, the board is soldered to a 1.5 mm. thick copper plate under high pressure. Two 0.75 mm. deep oval grooves are then cut using a 2.5 mm. diameter bore groove milling cutter for the source flanges of the two drive transistors. Countersinking is carried out for the LT1084CP voltage controller, with a precisely fitting opening for the TIM0910-4 transistor, in accordance with the dimension specified in the layout. The two components are then screwed directly onto the 8 mm. thick housing base. This provides exactly the height required for the stripline for the TIM0910-4. Following the preparation of the seven 2.1 mm. diameter bores for the screwing down and through-plating of the board in the housing and the tin-plating (or silver-plating) of the tracks, the board is

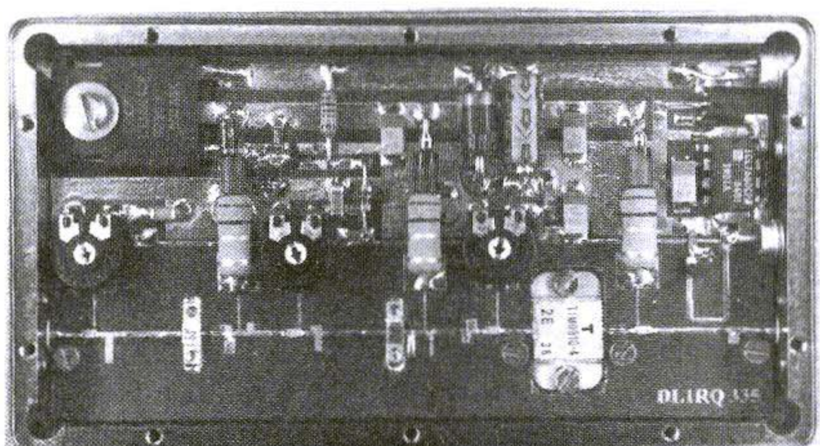
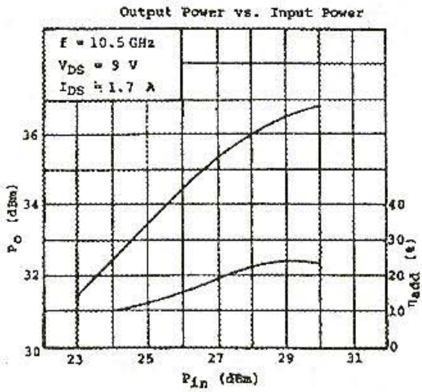


Fig.15: Example of a 5W Power Amplifier for 10 GHz



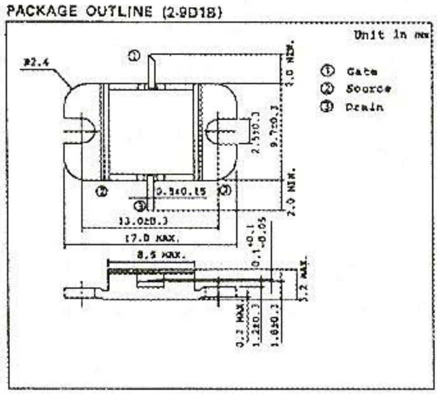
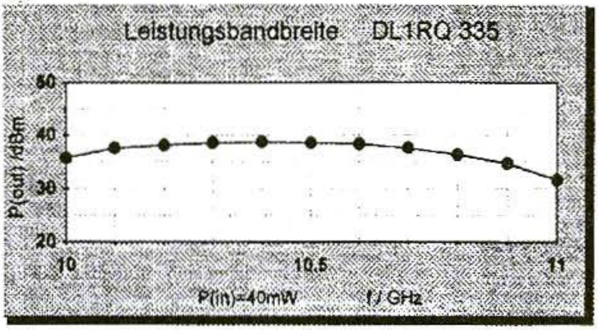


Fig.16: Power Data and Case Details for the Toshiba TIM0910-4 (7)

assembled, as far as the 10µF electrical capacitor (on the power supply bar), the LT1084CP and the three GaAs transistors (Fig.13). In order to guarantee good heat transmission between the copper plate and the housing, some heat-conducting paste is smeared onto the aluminium base in the area of the two drive transistors. Silver conductive lacquer can be smeared on to produce a good transition from the high-frequency section to the earth in the vicinity of the input, the output, the gate and the drain of the TIM0910-4. Of course, silver conductive lacquer must be applied extremely sparingly. Even a transient leak while the board is being screwed on can lead to considerable problems. (The author's prototype was tested without conductive lacquer. No difference could be detected from later versions with conductive lacquer!)

The partly-assembled board is now put into the housing, which has all the necessary bores, and is screwed down using seven M2 brass screws. When the LT1084CP has been incorporated (don't forget the little insulating discs!) and the connection to the feed-through capacitor has been completed, the DC function can be checked. All trimmers are pre-set to -1.5V for the gate voltage. The two drive transistors are soldered in just as already described for the 1Watt high-level stage. When the housing has cooled, the remaining components and the SMA bushes are mounted (with suitable Teflon collars). The final step is the incorporation of the "expensive bit", the TIM0910-4, into the opening provided in the board, using two M2 screws. Since a certain amount of lever action can not be excluded when the screws are tightened, the gate and drain lugs should not be soldered to the stripline until afterwards.

It is vital to bear in mind that, up until sometime early in 1993, Toshiba identified the drain lug by a chamfer. Since then, the gate lug has been chamfered. In case of doubt, a suitable Ohmmeter can be used for measurements. Battery-operated equipment with a low measuring voltage (< 0.5V) is suitable. The drain-source resistance is usually



Typical readings for a 5W Unit

Fig.17: Power Bandwidth

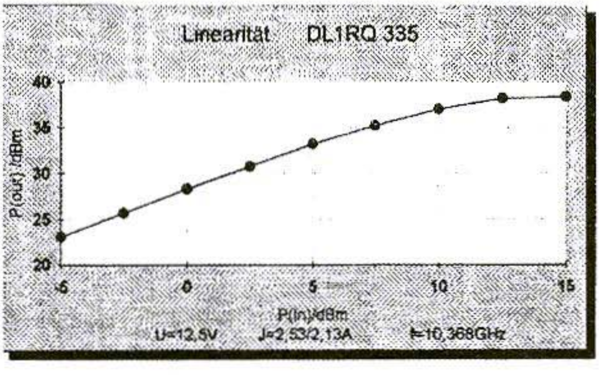


Fig.18: Linearity

markedly less than an Ohm. The gate-source resistance, by contrast, will be very high-ohmic - and this is irrespective of the polarity of the measurement voltage. Naturally, measurements must be carried out very carefully as static charges may be present. The author came to a decision as to whether to give preference during assembly to the best heat contact (by an abundant use of heat-conducting paste) or to the best high-frequency contact (by doing without the paste), in that (somewhat half-heartedly!) he applied less than a breath of this paste.

3.3. Calibration

First, the zero signal currents are set:

FSX52WF to approximately 80mA - this corresponds to a voltage drop of 800mV with a drain resistance of 10Ω; FLC103WG to app. 250mA - this corresponds to a voltage drop of 25mV with a drain resistance of 0.1Ω; TIM0910-4 to app. 2.0 A - this corresponds to a voltage drop of 200mV with a drain resistance of 0.1Ω. Should the readings not match the above values immediately, fine tuning should be carried out using the "small disc method".

3.4. Cooling

Estimating the cooling of the high-level stage we can calculate as follows:

App. Power loss for the TIM0910-4: $P_v = 9.5\ V * 2.1\ A \approx 20\ W$

The HF output is not taken into account!

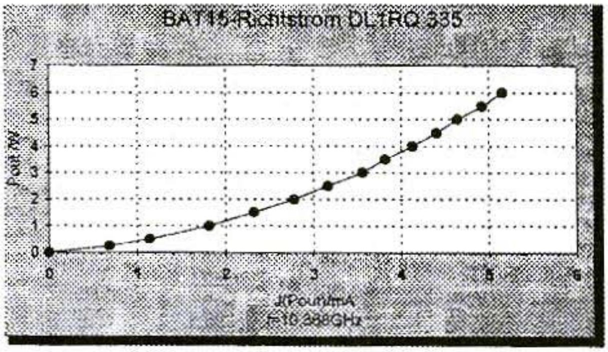


Fig.19: Relative Power Display using a BAT 15

Temperature differential between channel and flange:

$\Delta\varphi_{CC}$ = 3.5 K/W.20 W ≈ 70 K

i.e., a flange temperature of, for example, 60°C. gives a channel temperature of 130°C.. The maximum permissible channel temperature is 175°C.. If you want to "keep on the safe side", the high-level stage housing should be cooled in such a way that, even when the ambient temperature is at its most unfavourable (insolation!) a flange temperature of 60° C. will not be greatly exceeded at TIM0910-4.

I would like to thank all those who have contributed to this project. Special thanks go to my fellow radio-enthusiast Manfred Deutsch, DC4UI, who was always ready to help and advise me in selecting and testing components.

4. LITERATURE, REFERENCE SOURCES

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